Electronic Version
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[METHOD AND APPARATUS FOR IMPROVING CYCLE TIME IN A QUAD DATA RATE SRAM DEVICE]

Abstract

A method for implementing a self-timed, read to write operation in a memory storage device. In an exemplary embodiment, the method includes capturing a read address during a first half of a current clock cycle, and commencing a read operation so as to read data corresponding to the captured read address onto a pair of bit lines. A write operation is commenced for the current clock cycle so as to cause write data to appear on the pair of bit lines as soon as the read data from the captured read address is amplified by a sense amplifier, wherein the write operation uses a previous write address captured during a preceding clock cycle. A current write address is captured during a second half of the current clock cycle, said current write address used for a write operation implemented during a subsequent clock cycle, wherein the write operation for the current clock cycle is timed independent of the current write address captured during said second half of the current clock cycle.